Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said insulating film has a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound that includes silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film,

wherein said second insulating film is laminated on said first insulating film.

2. (Canceled).

3. (Previously Presented) A field-effect transistor according to claim 1, wherein the thickness of said first insulating film is not more than 150 nm.

4. (Previously Presented) A field-effect transistor according to claim 1, wherein a dielectric constant of said second insulating film is not more than 3.5.

5. (Previously Presented) A field-effect transistor according to claim 1,

wherein said insulating film including said multilayered film is formed while being separated from said gate electrode, and said second insulating film is provided between said first insulating film and said gate electrode.

6. (Previously Presented) A field-effect transistor according to claim 5, wherein said second insulating film is provided between said first insulating film and said gate electrode and said second insulating film is positioned below said field plate portion, and

said multilayered film including said first insulating film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode.

7. (Previously Presented) A field-effect transistor according to claim 1, further comprising a third insulating film on said second insulating film, the third insulating film being made of a compound that includes silicon and nitrogen as the constituent elements.

8. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said insulating film is made of a compound that includes silicon, nitrogen, and oxygen as constituent elements.

9. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating

film between said gate electrode and said drain electrode, and said insulating film has dielectric constants not more than 3.5.

10. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said gate electrode side of said insulating film between said gate electrode and said drain electrode is made of an insulating material having dielectric constants not more than 4, and said drain electrode side of said insulating film is made of an insulating material that includes silicon and nitrogen as constituent elements.

11. (Previously Presented) A field-effect transistor according to claim 10, wherein said drain electrode side of said insulating film is made of an insulating material that includes silicon, nitrogen, and oxygen as the constituent elements.

12. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field

plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween,

wherein a part of said insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound that includes silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film, and said gate electrode side is formed by a single-layer film of the first insulating film and said drain electrode side is formed by the multilayered film including said first insulating film and said second insulating film in said insulating film between said field plate portion and a surface of said semiconductor layer structure.

13. (Canceled).

14. (Canceled).

15. (Previously Presented) A field-effect transistor according to claim 1, wherein contact layers are arranged between said source electrode and a surface of said semiconductor layer structure and between said drain electrode and a surface of said semiconductor layer structure, respectively.

16. (Previously Presented) A field-effect transistor according to claim 15, wherein said contact layer is formed by an undoped AlGaN layer.

17. (Previously Presented) A field-effect transistor according to claim 16, wherein said field plate portion extends to an upper portion of said contact layer.

18. (Previously Presented) A field-effect transistor according to claim 1, wherein said semiconductor layer structure has a structure in which the channel layer made of InxGa1-xN ($0 \leq x \leq 1$), the electron supply layer made of AlyGa1-yN ($0 < y \leq 1$), and a cap layer made of GaN are sequentially laminate.

19. (Previously Presented) A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer,

wherein said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said insulating film has a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound that includes silicon and nitrogen as constituent elements, and said second insulating film having a dielectric constant lower than that of said first insulating film,

wherein a size of said field plate is not lower than 0.3 μm.

20. (Previously Presented) A field-effect transistor according to claim 19, wherein a size of said field plate is not lower than 0.5 μm.

21. (Previously Presented) A field-effect transistor according to claim 19, wherein a size of said field plate portion is not more than 70% of a distance between said gate electrode and said drain electrode.

22. (Previously Presented) A field-effect transistor according to claim 1, wherein said field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode.

23. (Previously Presented) A field-effect transistor according to claim 8, wherein said field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode.

24. (Currently Amended) A field-effect transistor according to claim 1, wherein said insulating film is formed having a double-stepped structure with first, second and third parallel regions in which the first parallel region is in contact with and disposed below the second parallel region, and in which the second parallel region is in contact with and disposed below the third parallel region~~, and in which the first and third parallel regions are not in contact with each other~~.